ABSTRACT OF THE DISCLOSURE

[0065] A transistor comprising a gate, a channel beneath the gate and separated from the gate by an insulator, a source adjacent to the channel on a first side of the gate, a drain adjacent to the channel on a second side of the gate, doped extension regions into the channel from the source and the drain that underlap the gate, and insulating spacers adjacent to sidewalls of the gate that overlap the extension regions. The insulating spacers may be used to align the doped extension regions, offset the extension regions from the gate, and reduce Miller capacitance and standby leakage current.